

MS-7037

Version 200
03/29/2004 Update

Intel (R) Springdale (GMCH) + ICH5 Chipset
Intel Northwood & Prescott mPGA478B Processor

CPU:

Intel Northwood/Prescott - 3.6G & Above

System Chipset:

Intel Springdale - GMCH (North Bridge) 848P
Intel ICH5 (South Bridge)

On Board Chipset:

CLOCK -- Cypress CY28405

On Board Chipset:

BIOS -- FWH EEPROM 4M

AC'97 Codec -- REALTEK / ALC655

LPC Super I/O -- W83627THF

LAN - REALTEK RTL8110S/8100C

1394 - VIA 6307

Main Memory:

DDR * 2

Expansion Slots:

PCI2.3 SLOT * 3

AGP4X/8X SLOT * 1

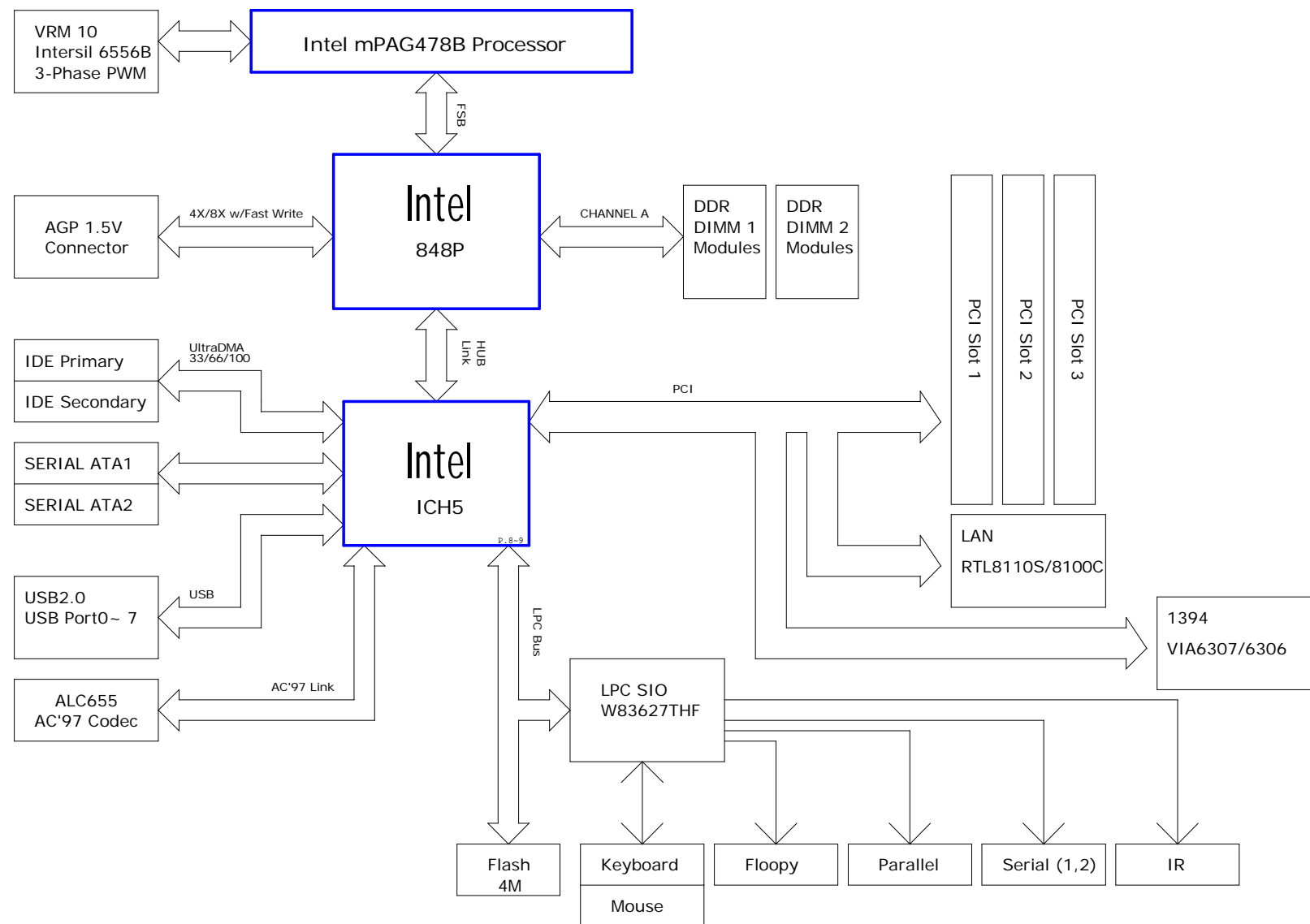
ST PWM:

Controller: ST6710

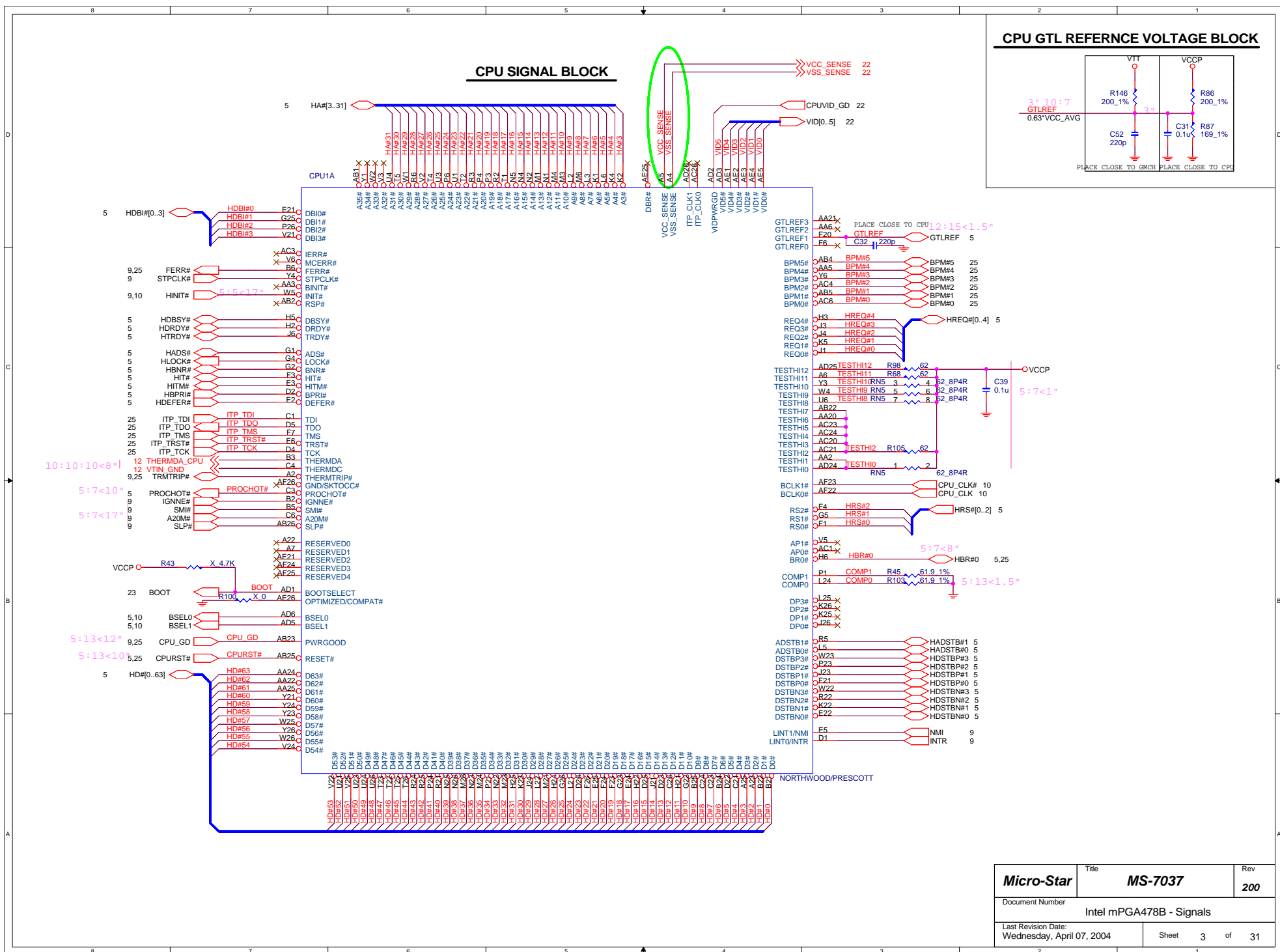
ERP BOM	Function Description	
501/601-7037	Opt : STD	848P+ICH5,W/LAN-8100,W/655,W/1394-6307
05S---		

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Block Diagram

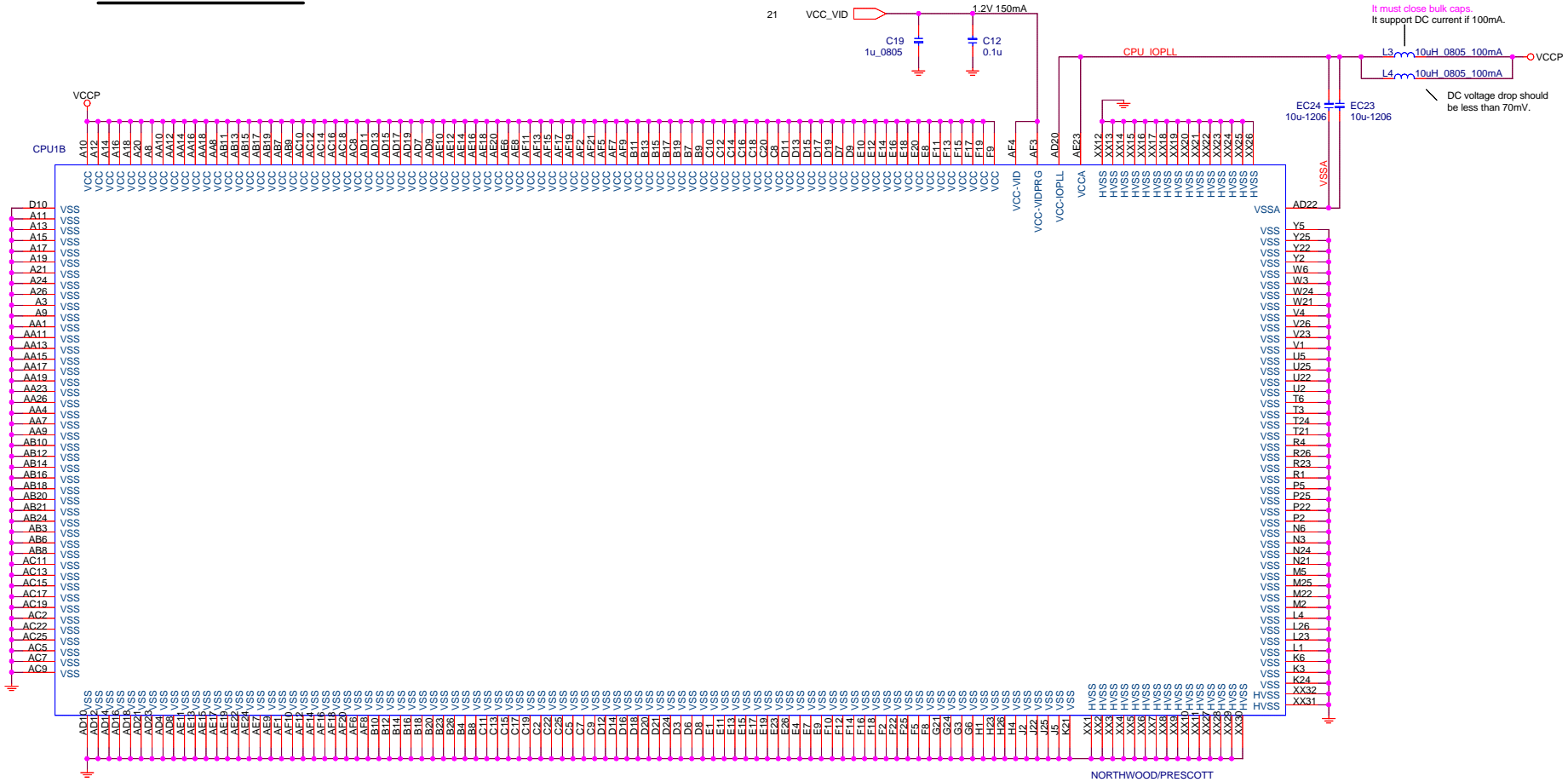


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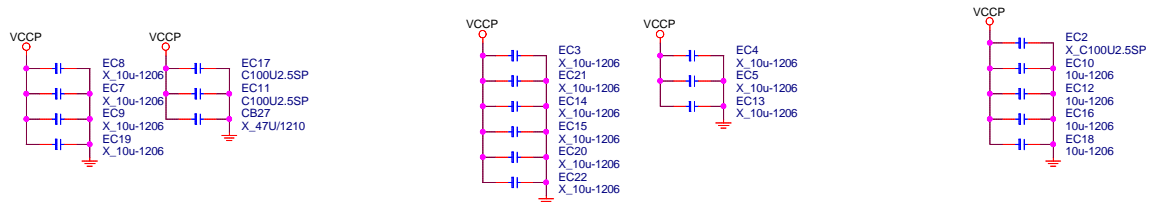


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Document Number Intel mPGA478B - Signals		
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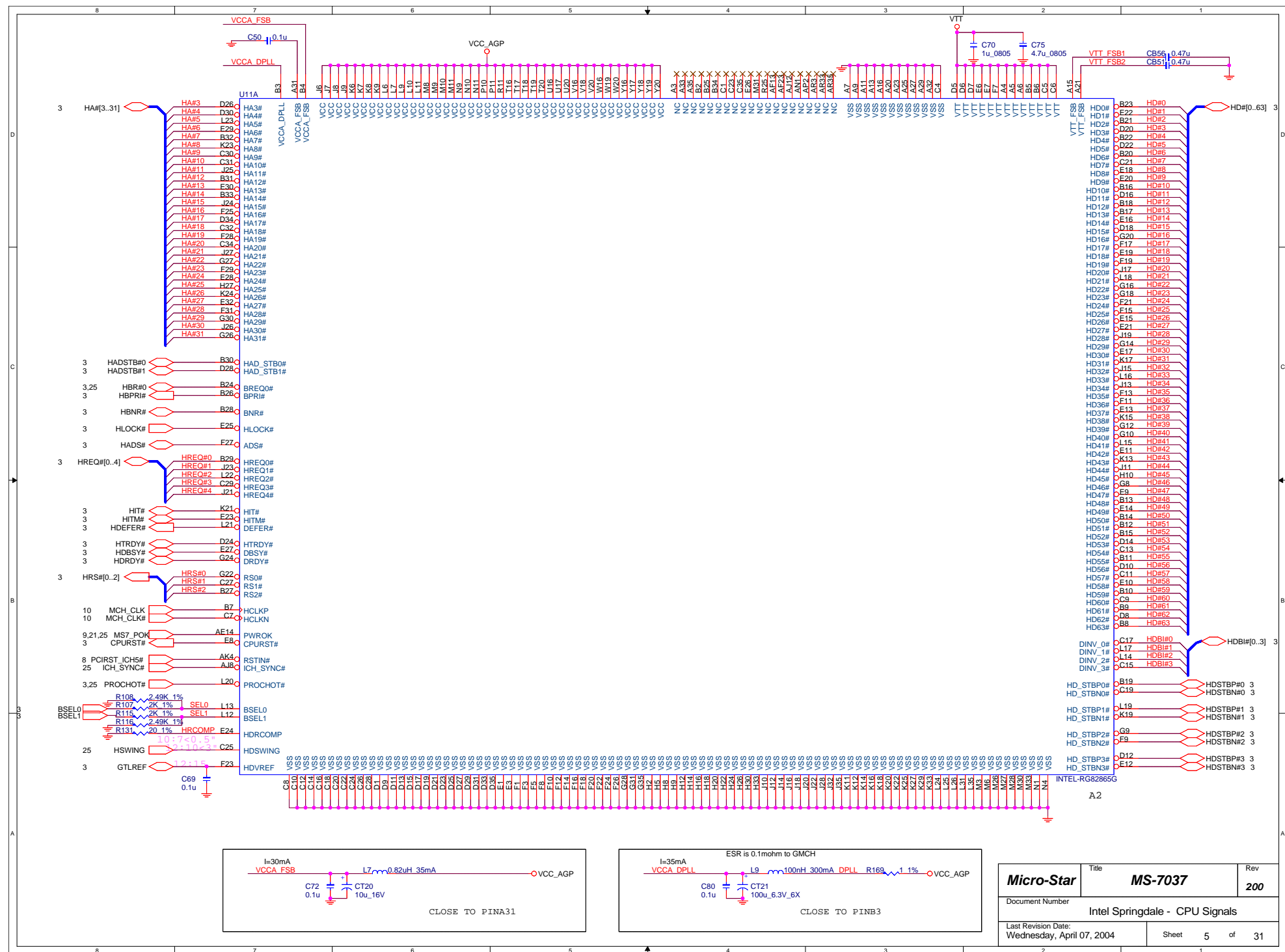
CPU VOLTAGE BLOCK

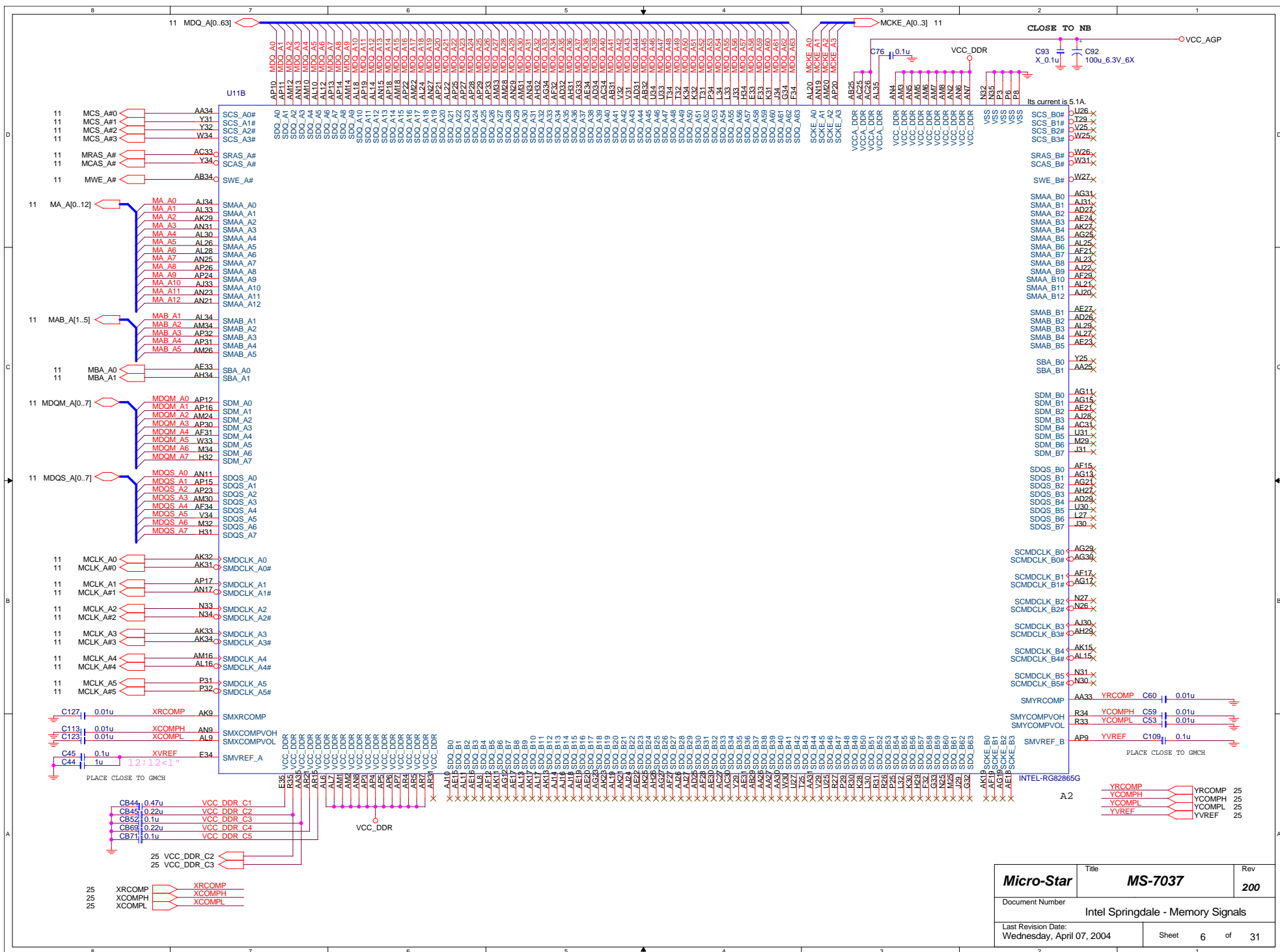


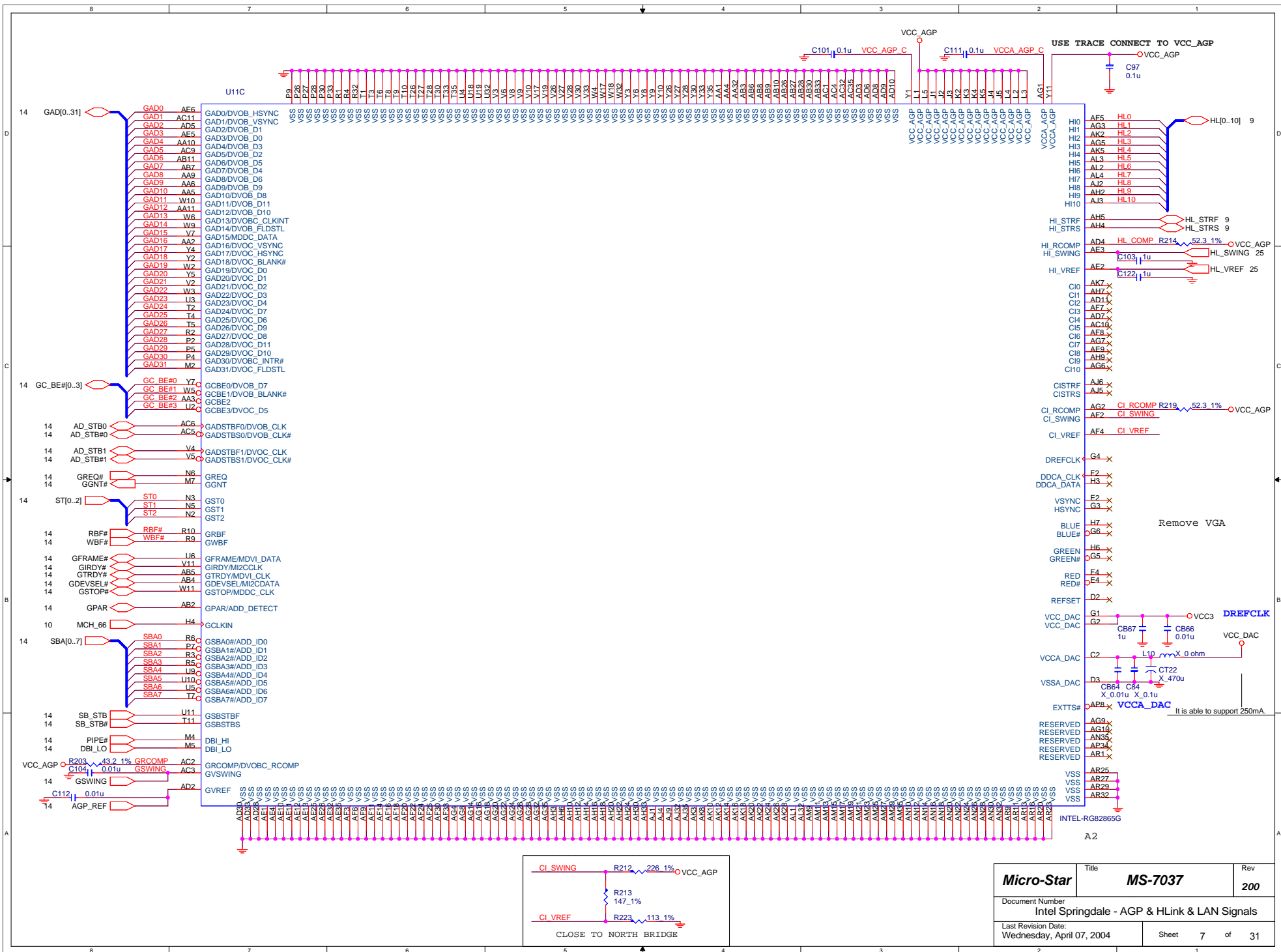
CPU DECOUPLING CAPACITORS



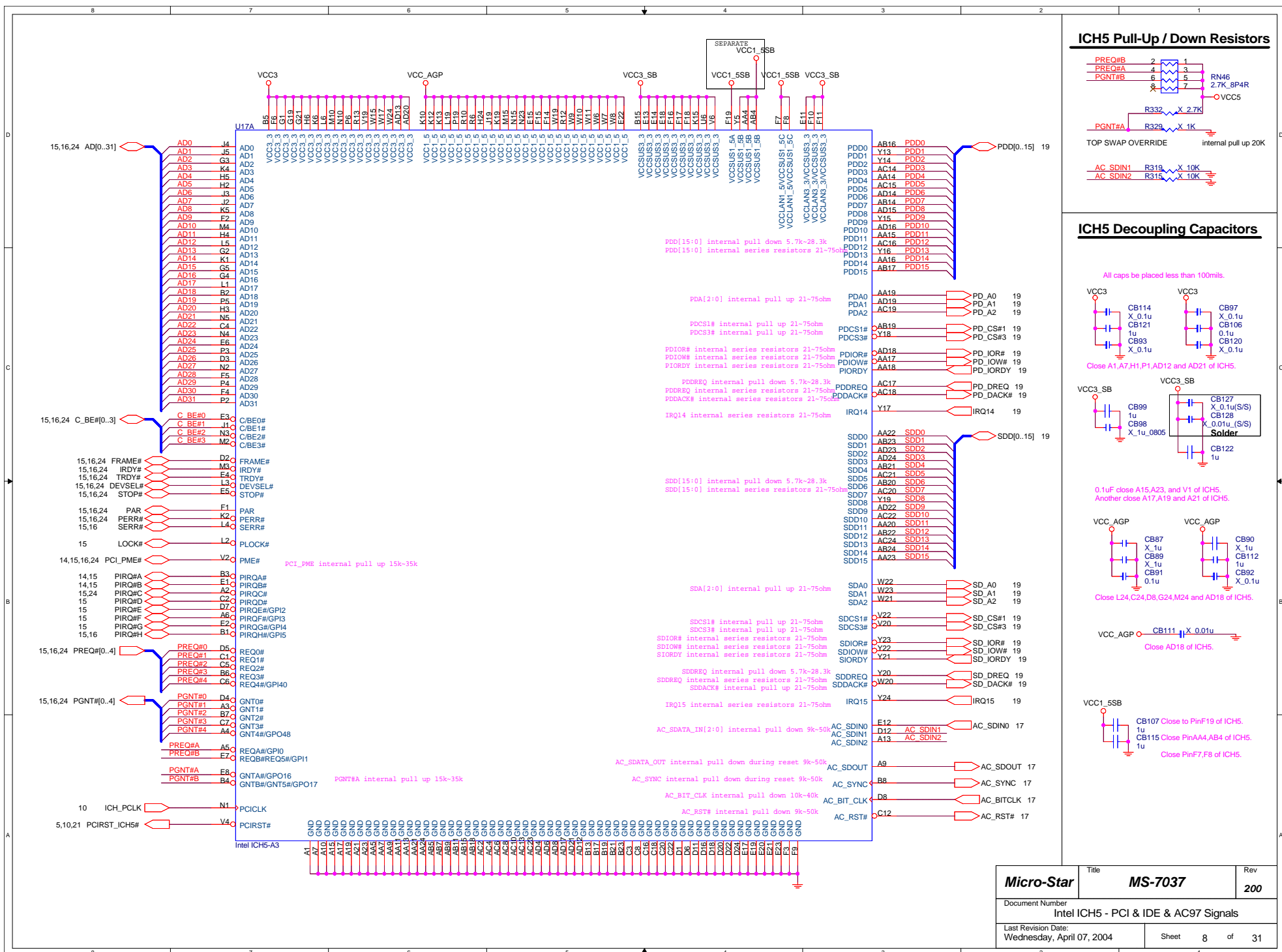
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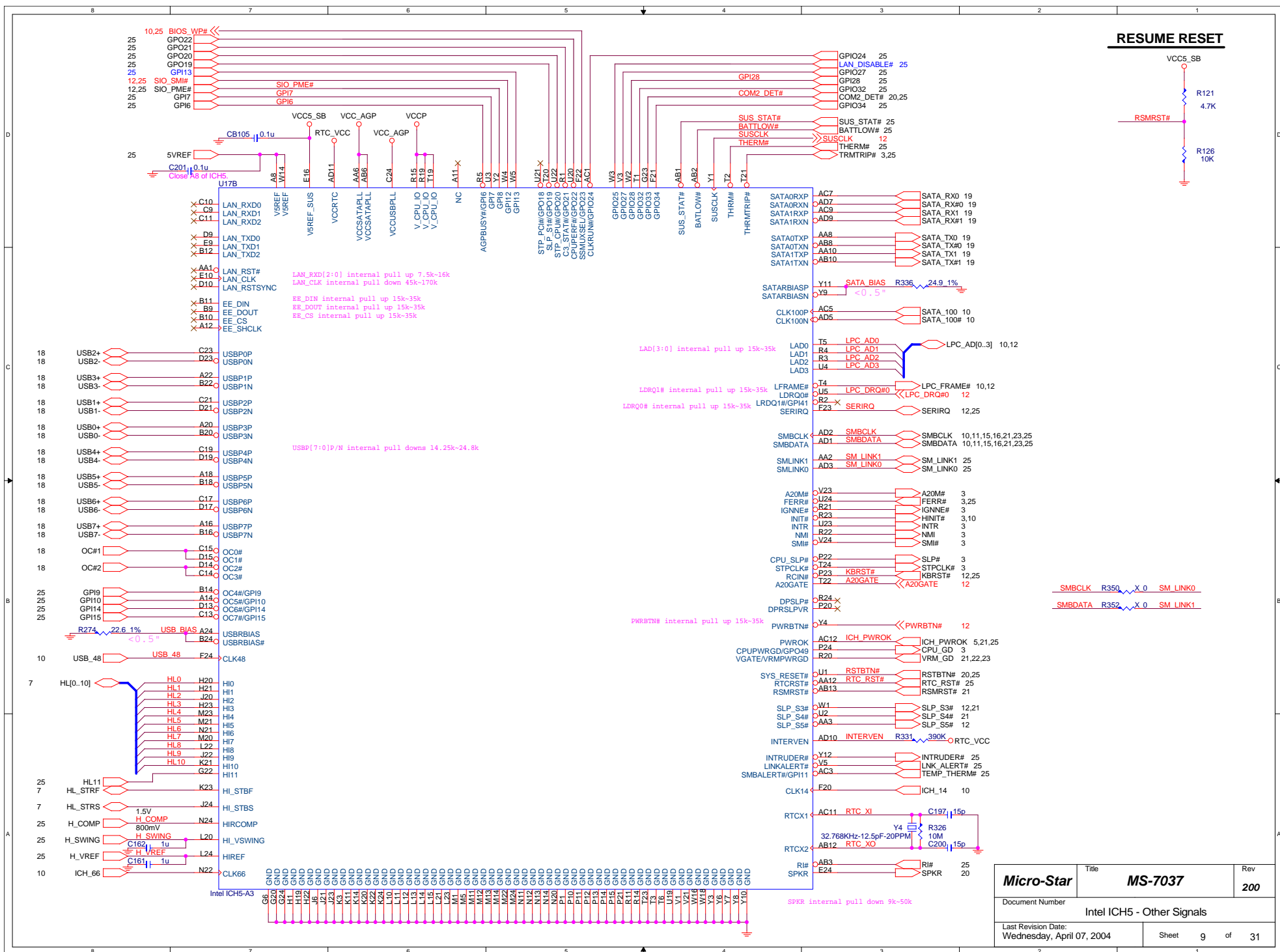




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	Document Number	Intel Springdale - AGP & HLink & LAN Signals		
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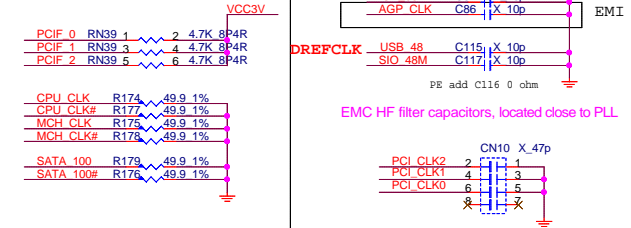
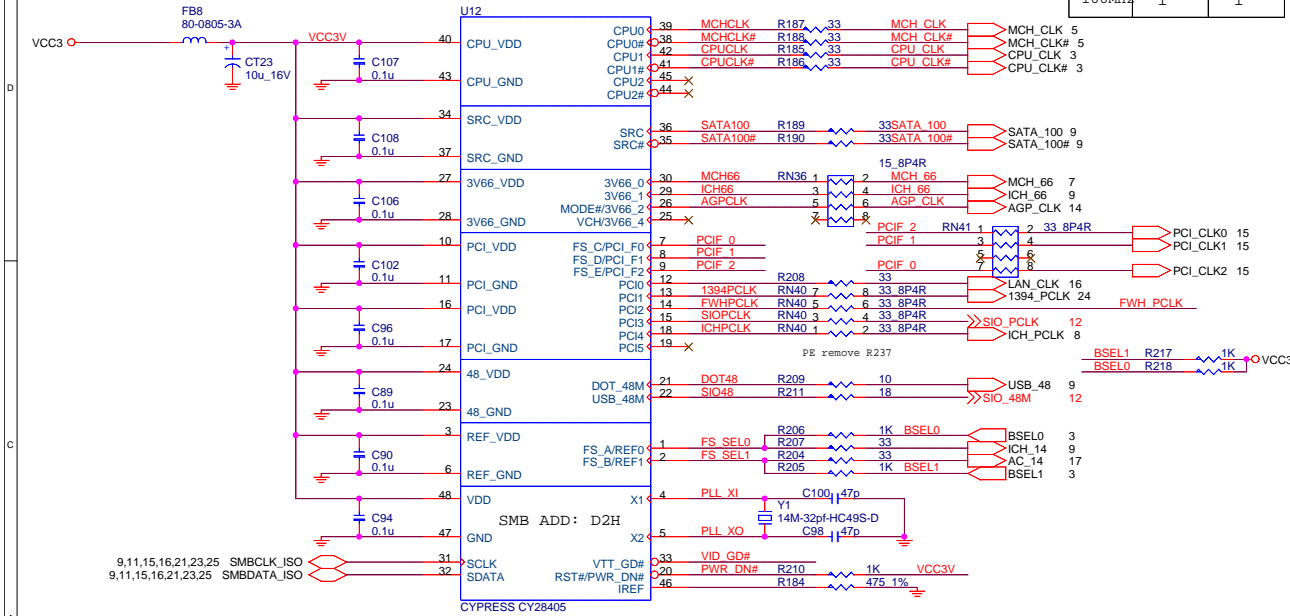


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Intel ICH5 - PCI & IDE & AC97 Signals				
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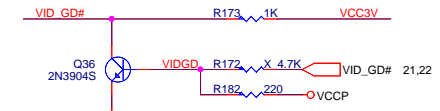


Micro-Star	Title MS-7037	Rev 200
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Intel ICH5 - Other Signals		
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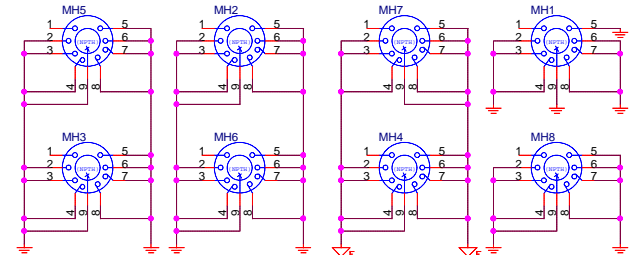
CLOCK GENERATOR



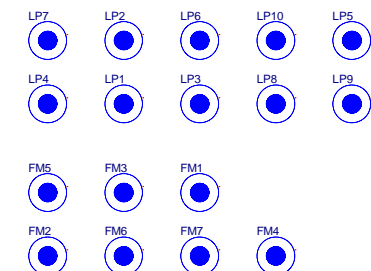
CLOCK GENERATOR VTT POWER DOWN BLOCK



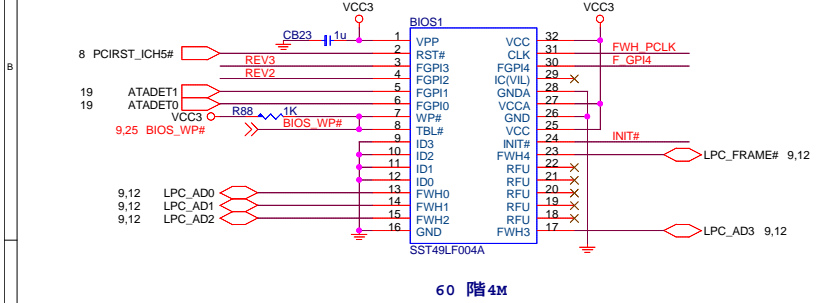
Mounting Holes



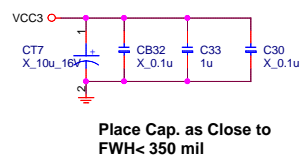
Optics Orientation Holes



FIRMWARE HUB (FWH)

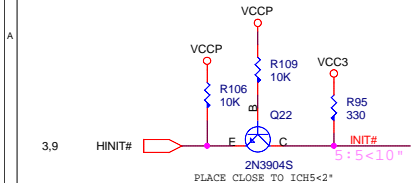


FWH DECOUPLING CAPACITORS

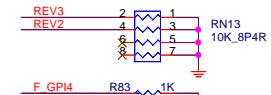


Place Cap. as Close to FWH< 350 mil

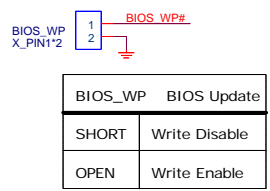
FWH INIT Signal Voltage Translation



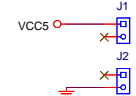
FWH RESISTORS



FWH write protect



Simulation



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DDR DIMM1

DDR DIMM2

DDR Terminational Resistors

SIGNALS

SIGNALS

POWER

POWER

DECOUPLING CAPACITORS

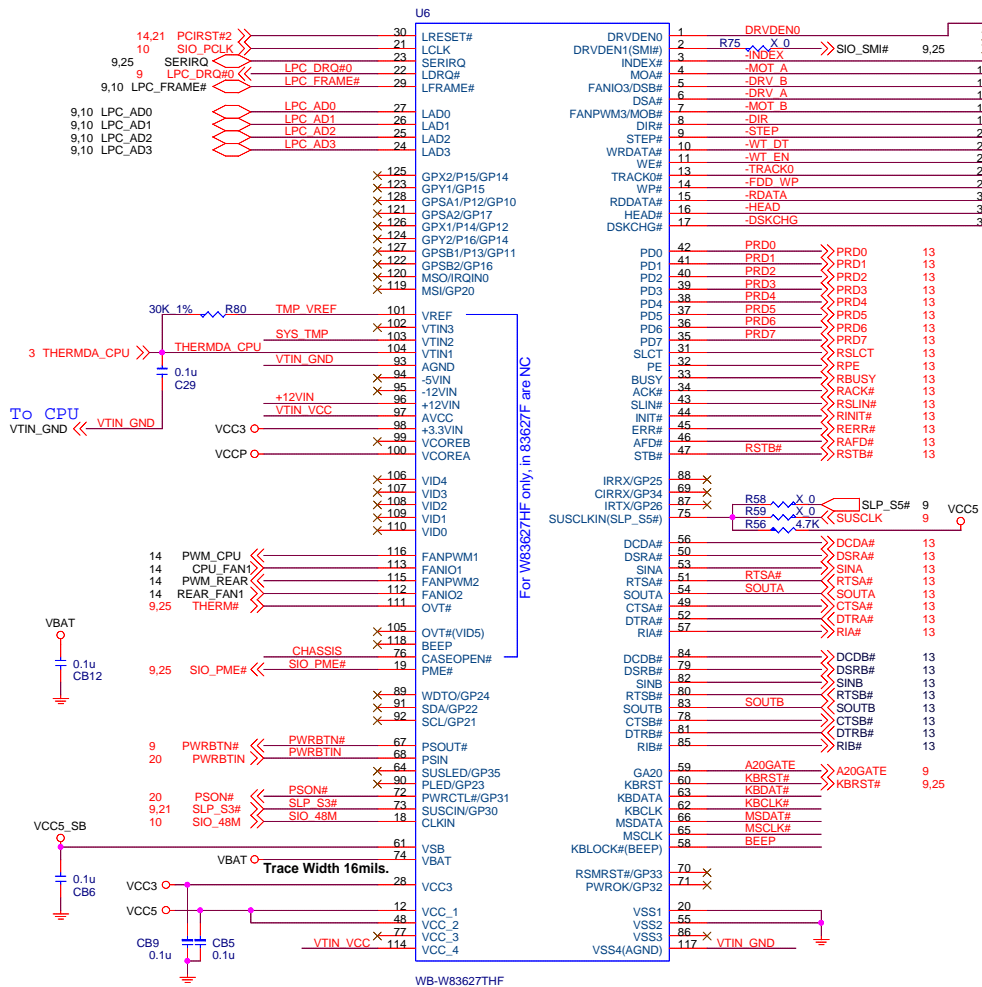
DECOUPLING CAPACITORS

ADDR.=1010000B(A0H)

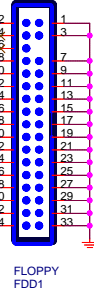
ADDR.=1010001B(A2H)

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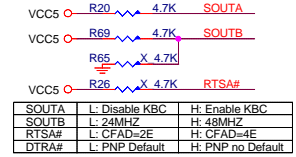
LPC SUPER I/O W83627THF



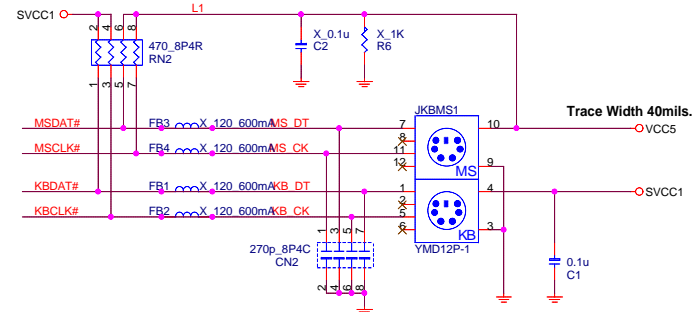
FLOPPY CONNECTOR



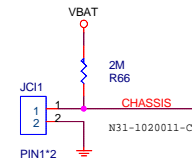
SUPER I/O STRAPPING RESISTOR



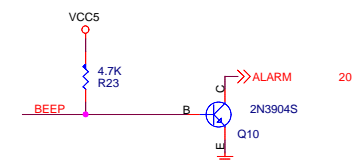
PS2 KEYBOARD & MOUSE CONNECTOR



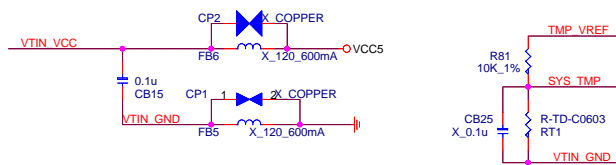
Chassis Intrusion



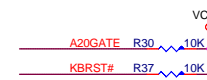
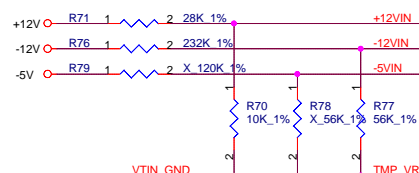
SPEAKER BLOCK



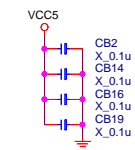
THERMAL RESISTOR BLOCK



NOTE: LOCATE CLOSE STATUS PANEL

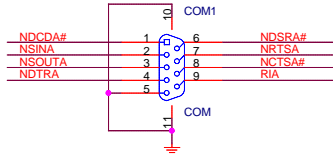
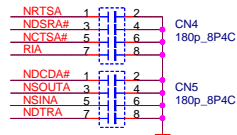
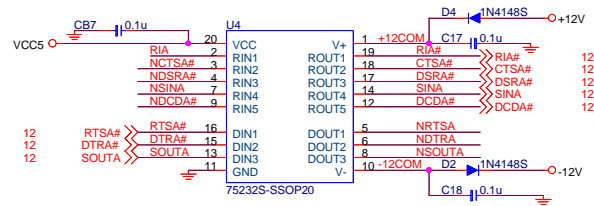


LPC I/O DECOUPLING CAPACITORS

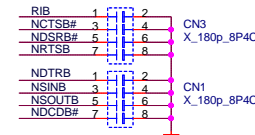
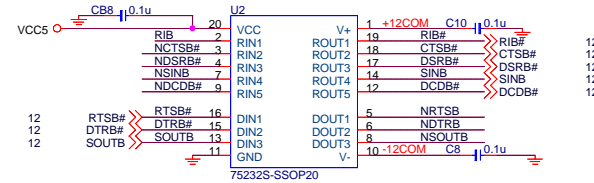


Micro-Star	Title	MS-7037	Rev	200
Document Number	SIO-W83627HF & KB/MS & FDD			
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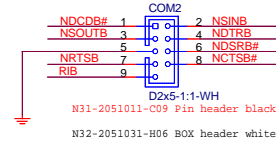
SERIAL PORT 1



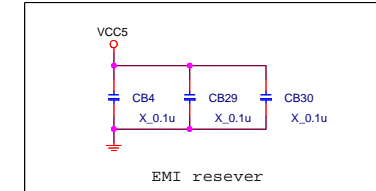
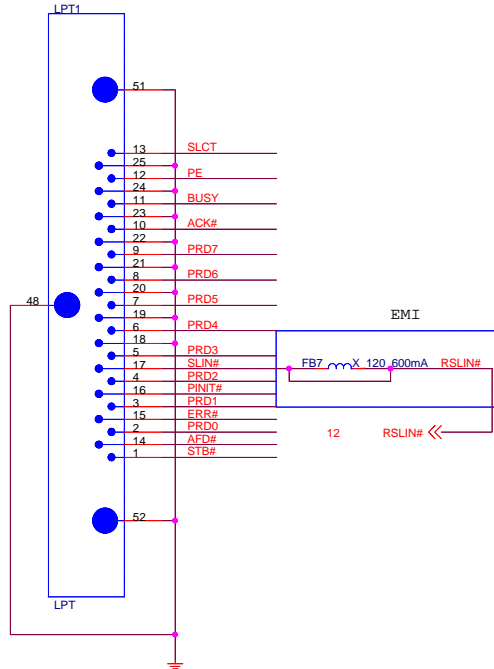
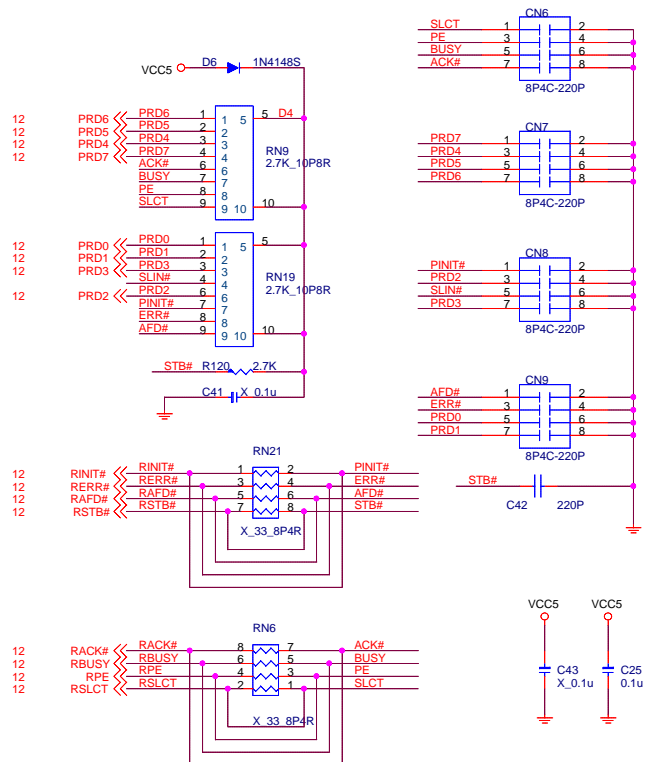
SERIAL PORT 2



COM2 HEADER



PARALLAL PORT



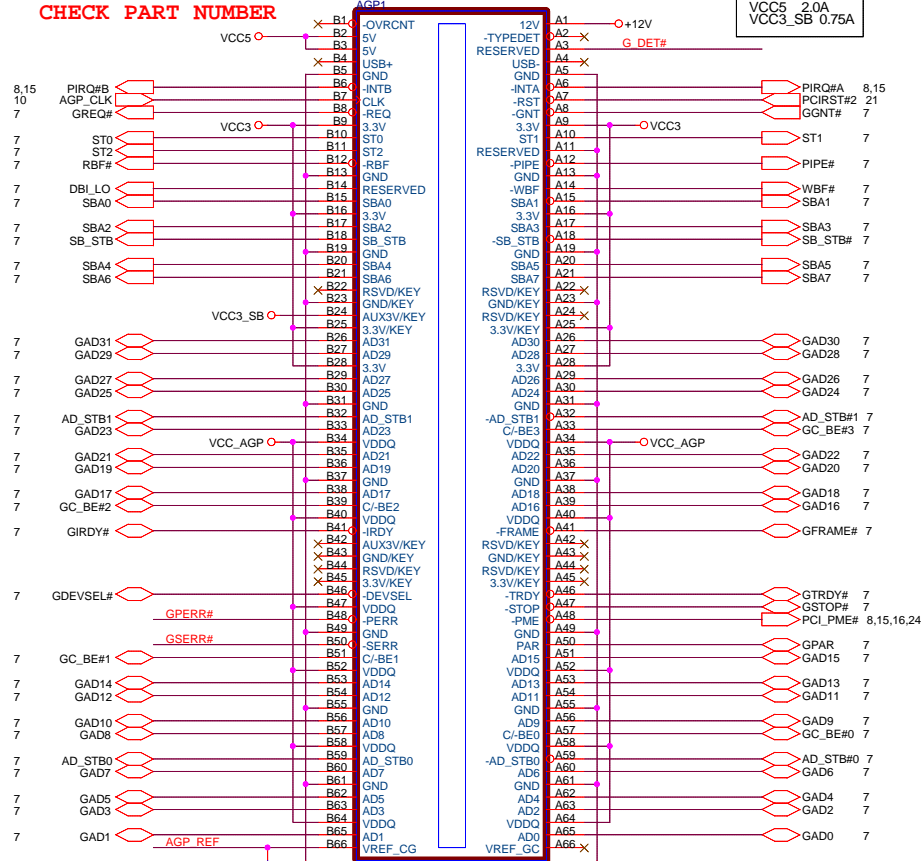
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AGP 1.5V 1X/2X/4X/8X SLOT(AGP VER:3.0)

VCC5 = 60mils trace / 15 mils space

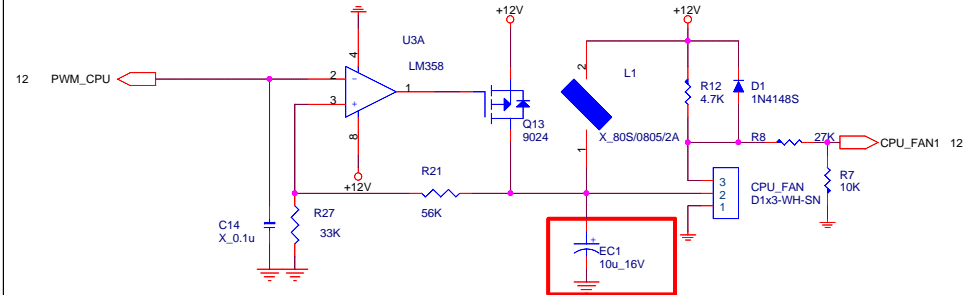
CHECK PART NUMBER

AGP Slot Imax
VCCg 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A
VCC3_SB 0.75A

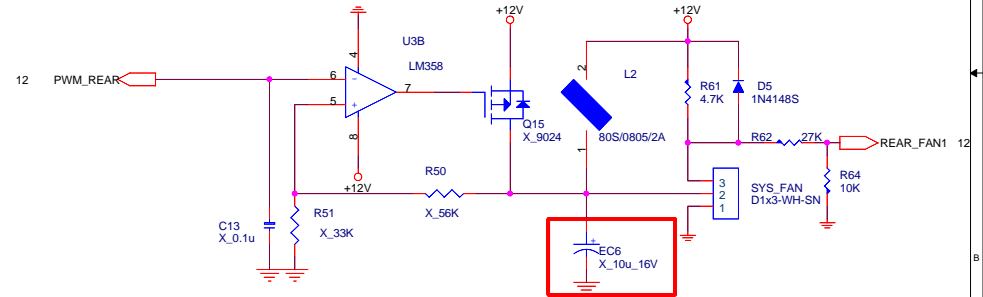


PIRQ#A / PIRQ#B

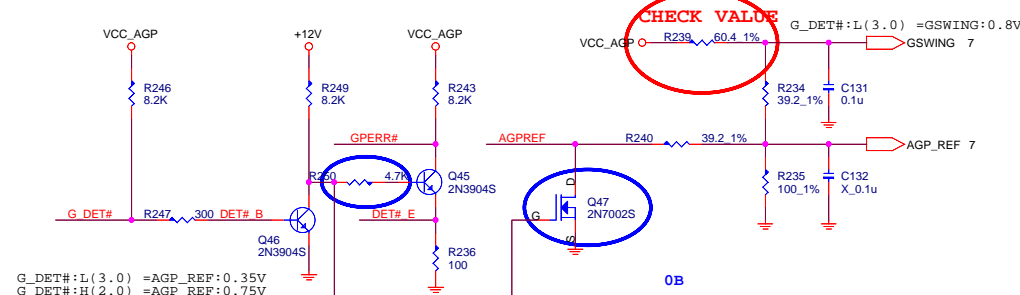
CPU FAN



SYSTEM FAN



Springdale Reference & Swing Voltage Circuit

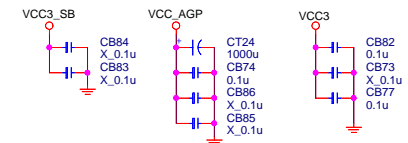


AGP TERMINATION RESISTORS

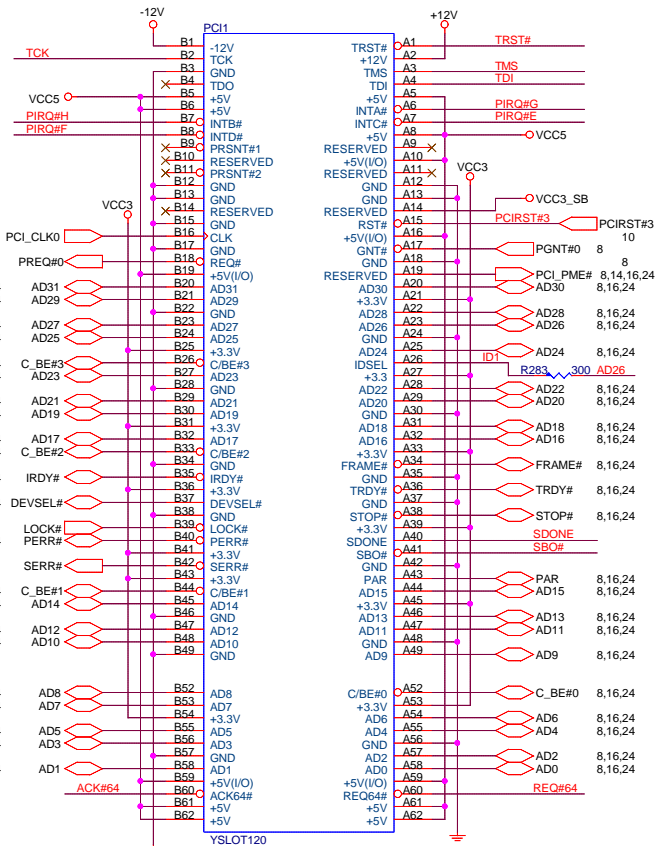
GSERR# R237 8.2K VCC_AGP

LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.
Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



Micro-Star	Title	MS-7037	Rev	200
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The diagram illustrates the pin-to-pin compatibility between the YSLOT120 and YSLOT120T headers. It shows two columns of pins, one for YSLOT120 (left) and one for YSLOT120T (right). Each pin is labeled with its number and function. The functions are color-coded: red for power and ground, blue for control and status, green for data and address, and yellow for peripheral functions. The diagram shows that the two pin headers are pin-to-pin compatible, with the same pin numbers and functions on both sides.

YSLOT120 Pin	YSLOT120T Pin	Function
B1	A1	TRST#
B2	A2	TCK
B3	A3	TMS
B4	A4	TDI
B5	A5	TDI
B6	A6	PIRQ#F
B7	A7	PIRQ#H
B8	A8	PIRQ#
B9	A9	VCC5
B10	A10	RESERVED
B11	A11	RESERVED
B12	A12	GND
B13	A13	GND
B14	A14	RESERVED
B15	A15	RESERVED
B16	A16	RESERVED
B17	A17	RESERVED
B18	A18	RESERVED
B19	A19	RESERVED
B20	A20	RESERVED
B21	A21	RESERVED
B22	A22	RESERVED
B23	A23	RESERVED
B24	A24	RESERVED
B25	A25	RESERVED
B26	A26	RESERVED
B27	A27	RESERVED
B28	A28	RESERVED
B29	A29	RESERVED
B30	A30	RESERVED
B31	A31	RESERVED
B32	A32	RESERVED
B33	A33	RESERVED
B34	A34	RESERVED
B35	A35	RESERVED
B36	A36	RESERVED
B37	A37	RESERVED
B38	A38	RESERVED
B39	A39	RESERVED
B40	A40	RESERVED
B41	A41	RESERVED
B42	A42	RESERVED
B43	A43	RESERVED
B44	A44	RESERVED
B45	A45	RESERVED
B46	A46	RESERVED
B47	A47	RESERVED
B48	A48	RESERVED
B49	A49	RESERVED
B50	A50	RESERVED
B51	A51	RESERVED
B52	A52	RESERVED
B53	A53	RESERVED
B54	A54	RESERVED
B55	A55	RESERVED
B56	A56	RESERVED
B57	A57	RESERVED
B58	A58	RESERVED
B59	A59	RESERVED
B60	A60	RESERVED
B61	A61	RESERVED
B62	A62	RESERVED

Pin-to-pin connection diagram for the AD9080 evaluation board. The diagram shows two columns of pins, one for the AD9080 (left) and one for the evaluation board (right). Pins are numbered B1 through B62. Connections are indicated by lines and labels. Power pins are connected to -12V and +12V. Signal pins are connected to various board signals like TCK, TMS, TDI, PIRQ#E, PIRQ#G, VCC5, VCC3, PCIRST#3, PGNT#2, PCI_PME#, AD30, AD28, AD26, AD24, ID3 R348, AD22, AD20, AD18, AD16, FRAME#, TRDY#, STOP#, SDONE, SBO#, PAR, AD15, AD13, AD11, AD9, C BE#0, AD6, AD5, AD4, AD3, AD2, AD0, REQ#64, ACK#64, and VSLT120. Some pins are marked with 'X' indicating a connection. A note '300 AD28' is present near pin AD28.

FRAME# 2 1 VCC5
IRDY# 4 3
TRDY# 6 5 RN42
DEVSEL# 8 7 2.7K_8P4R

8 8.24
STOP# 2 1 VCC5
LOCK# 4 3
PERR# 6 5 RN45
SERR# 8 7 2.7K_8P4R

VCC5 VCC3
CB110 X 0.1u
CB78 X 0.1u

PREQ#2 2 1 VCC5
PREQ#0 4 3
PREQ#1 6 5 RN49
PREQ#3 8 7 2.7K_8P4R

PREQ#4 R330 2.7K

REQ#64 R285 4.7K VCC5
ACK#64 R286 4.7K

TMS R364 X 4.7K
TDI R365 X 4.7K

TCK R345 X 4.7K
TRST# R346 X 4.7K

SDONE SMBCLK 9,10,11,16,21,23,25

SBO# SMBDATA 9,10,11,16,21,23,25

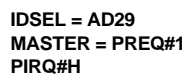
Schematic diagram of the power supply section of the MS-3037. The diagram shows five power rails and their associated capacitors:

- VCC5:** Connected to a series of capacitors: CB109, CB80, CB96, CB104, CB94, and CB119.
- VCC3:** Connected to a 1000uF electrolytic capacitor (CT29) in series with capacitors CB116, CB118, CB65, CB103, and CB102.
- 12V:** Connected to a 10uF electrolytic capacitor (CT27) in series with capacitor CB123.
- +12V:** Connected to a 10uF electrolytic capacitor (CT28) in series with capacitors CB124, CB81, and CB108.
- VCC3.5B:** Connected to a series of capacitors: CB100, CB95, CB117, CB101, and CB101.

Title	Rev
MS-3037	

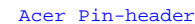
<i>Micro-Star</i>	Title <i>MS-7037</i>	Rev <i>200</i>
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R287 2.49K for 8110S; 5.6k for 8100C



	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8100C	2.5V	2.5V	3.3V	X	2.5V
8110S	1.8V	1.8V	2.5V	3.3V	X

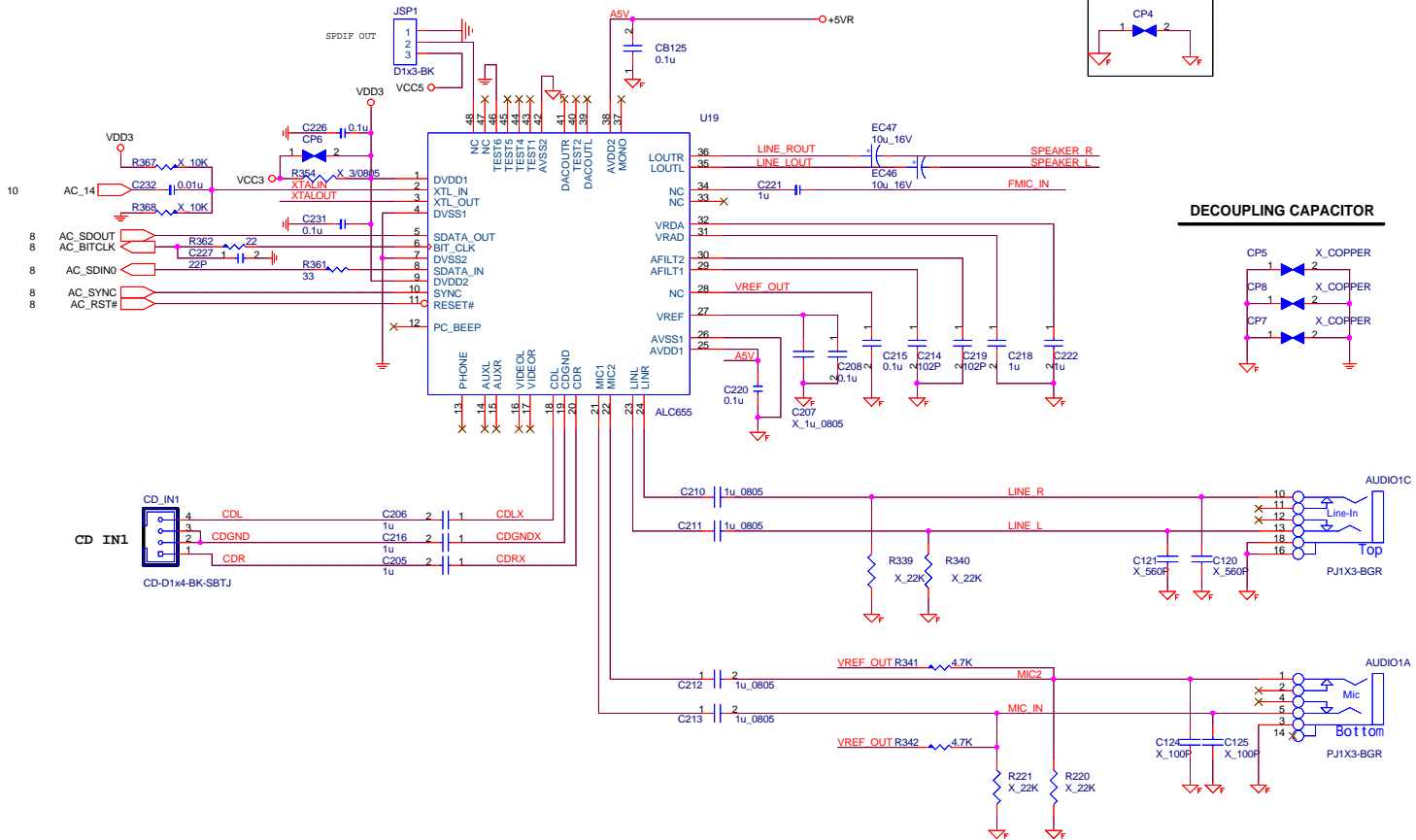




```
GbE: 8110S LAN(1000M)
TE: 8100C LAN(10/100M)
L: With LAN option
X: No Stuff
```

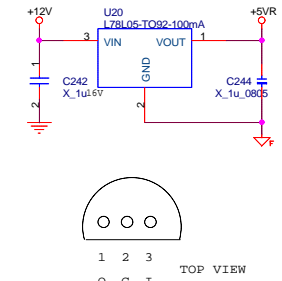
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Document Number LAN RTL8110S/8100C		
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ALC655 AC97 CODEC

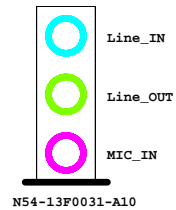
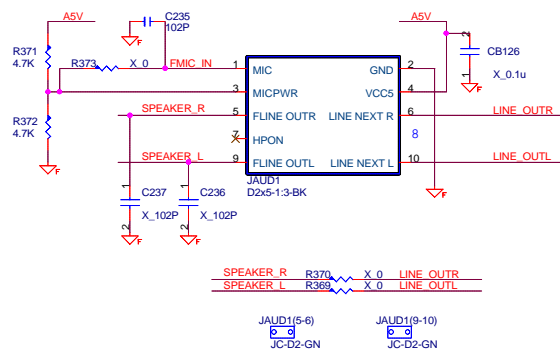


AUDIO CODE REGULATORS

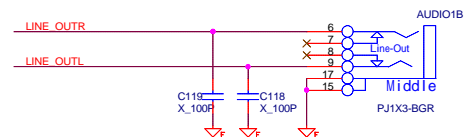
Trace Width 30mils.



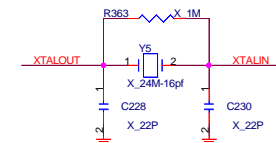
Intel Front Audio Connector



SPEAKER OUT JACK



AUDIO CODE CRYSTAL CIRCUIT



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Diagram of the NEAR USB CONNECTOR. The connector is labeled JUSB1 and has pins 1 through 10. The connections are as follows:

- USB4- (pin 9) connects to SBD4- (pin 1)
- USB4+ (pin 9) connects to SBD4+ (pin 2)
- USB5- (pin 9) connects to SBD5- (pin 3)
- USB5+ (pin 9) connects to SBD5+ (pin 4)
- SVCC2 (pin 2) connects to pin 2 of JUSB1
- OC#2 (pin 10) connects to pin 10 of JUSB1

[illegible]

9 USB6+ SBD6+

9 USB6- SBD6-

9 USB7+ SBD7+

9 USB7- SBD7-

JUSB2

1 2

3 4

5 6

7 8

10 10

CON2X5-1_Y

SVCC2

SBD6+

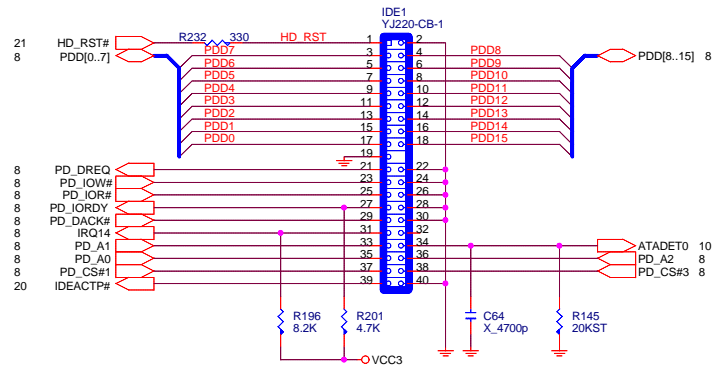
SBD7-

SBD7+

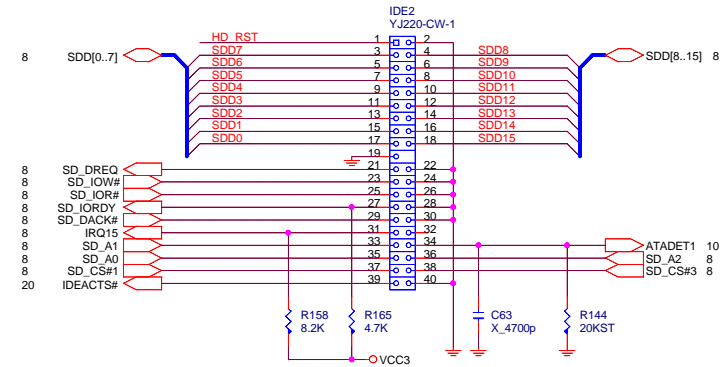
OC#2

NEAR USB CONNECTOR

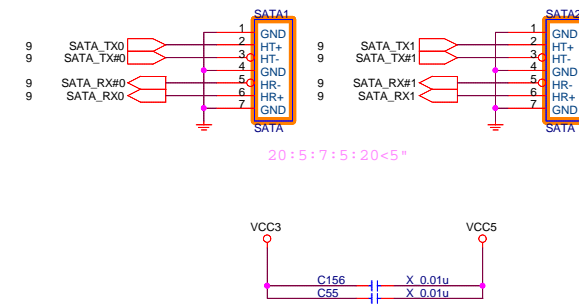
PRIMARY IDE BLOCK



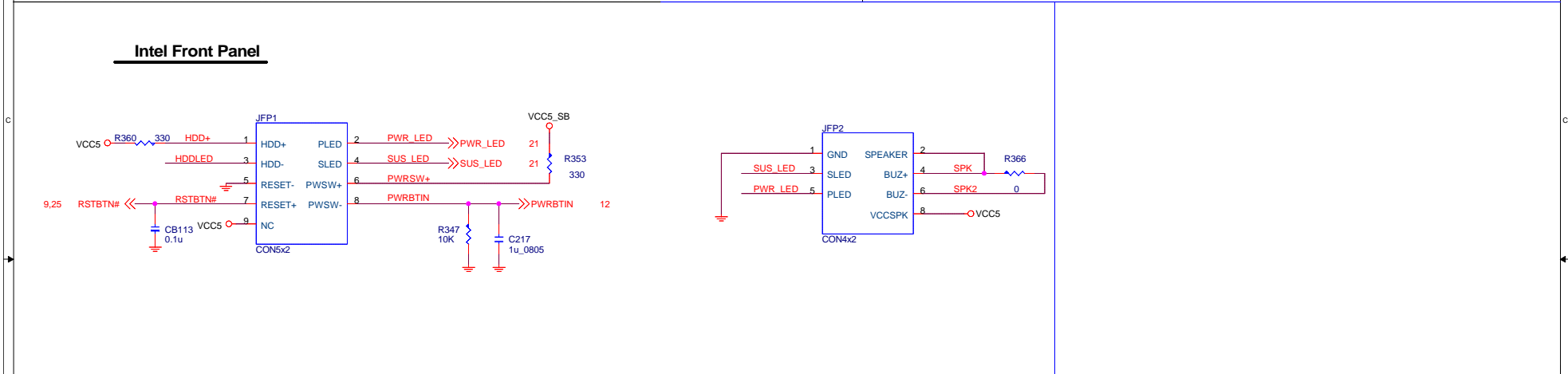
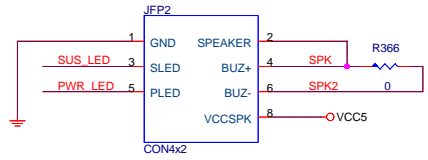
SECONDARY IDE BLOCK



SERIAL ATA CONNECTOR BLOCK



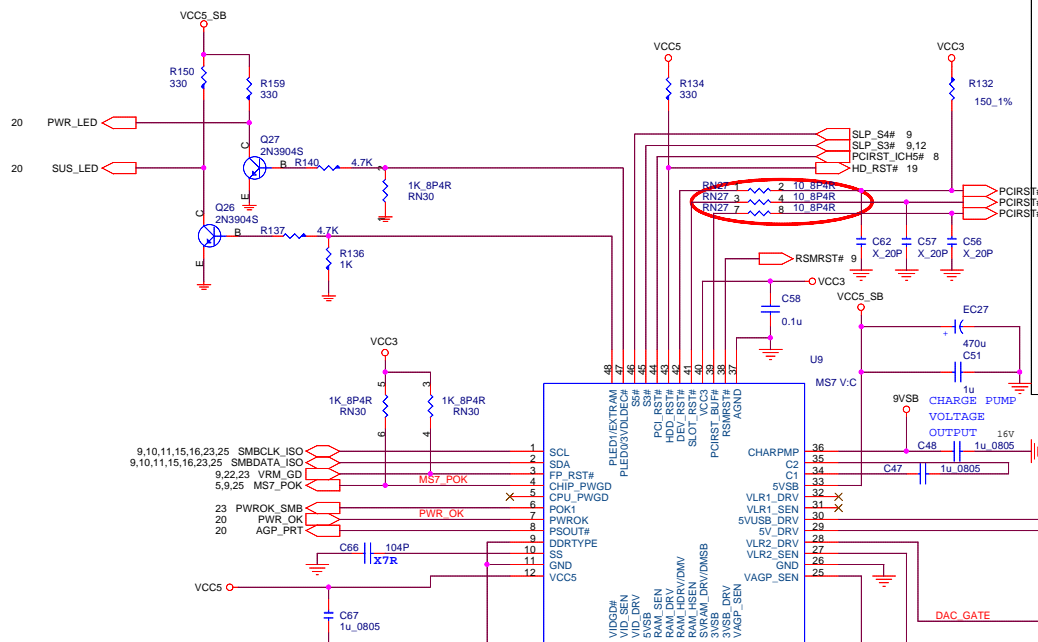
Micro-Star	Title	MS-7037	Rev	200
	Document Number	IDE & SATA & Game port		
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[illegible]

ACPI Controller

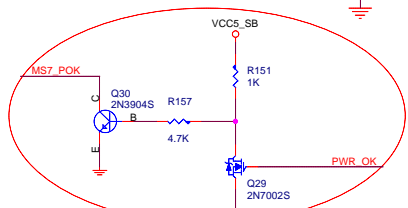
ICH5 300mA
PCI 375+20+20= 415mA
VCC3_SB 715mA

1.7V@250mA				
Power	S0	S3	S5	
VCC3_SB	Main	Standby	Standby	
VCC5_STR	Main	Standby	0V	
MEM_STR	Main	Standby	0V	



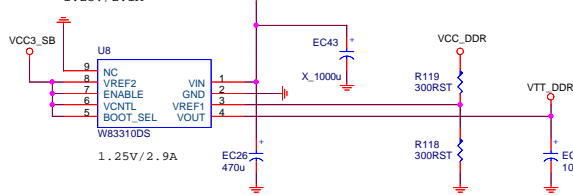
VCC3_VID/VID_GOOD

Place MOSFET near CPU



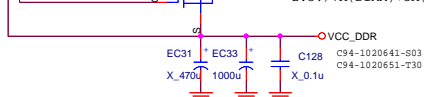
DDR VTT Power

1.25V/2.1A

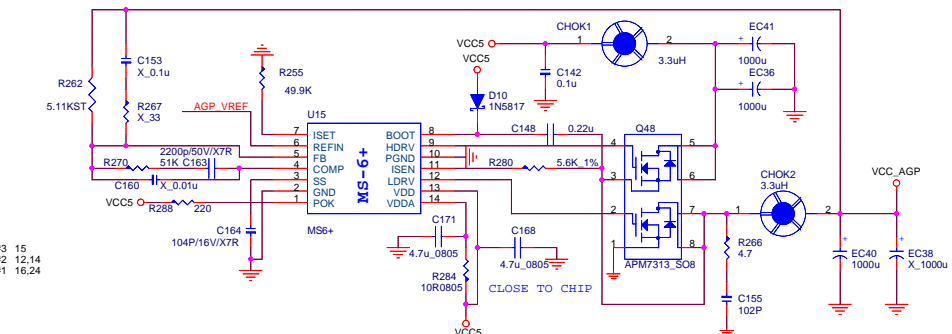


DDR 2.5V Power

2.5V/7A (DIMM) + 5A (NB)

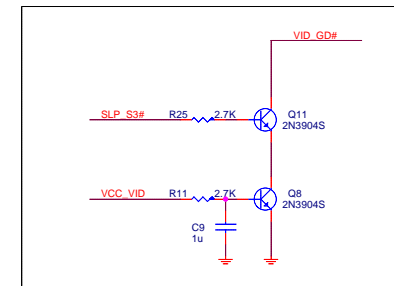
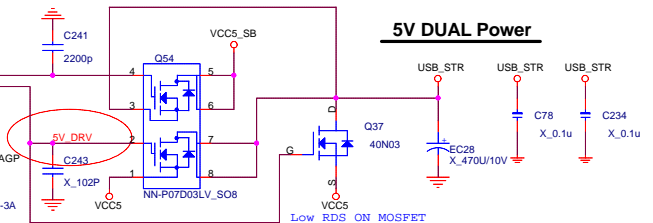


AGP POWER

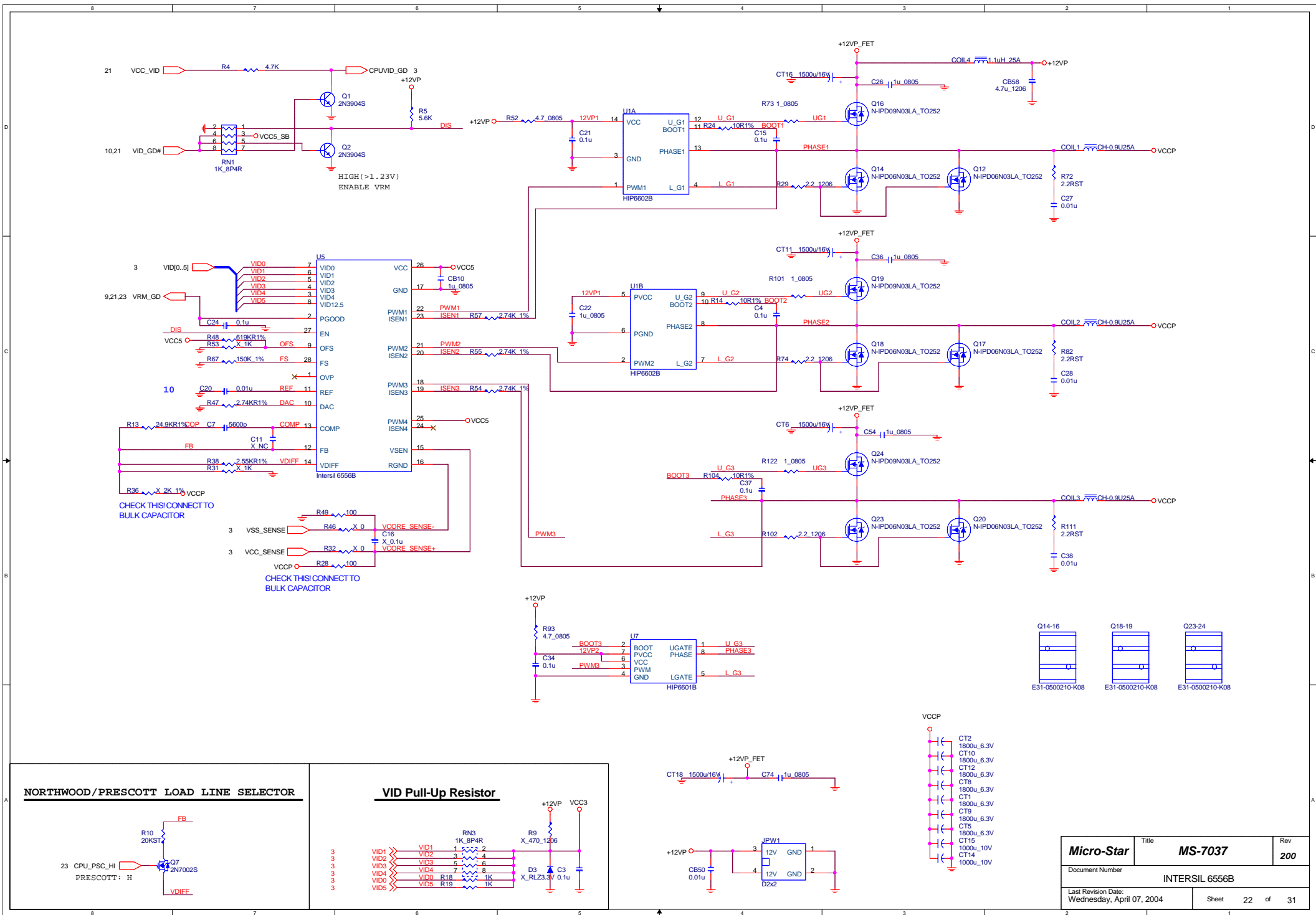


$I_o \times R_{ds(on)} = I_{sen}(72\mu A) \times R_{sen}$
 $I_d = 6A, I_d(max) = 24A$
 $R_{ds(on)}/10V = 21m\ ohm \sim 28m\ ohm$
 $Overcurrent\ (4.7K\ ohm) = 12A \sim 16A$

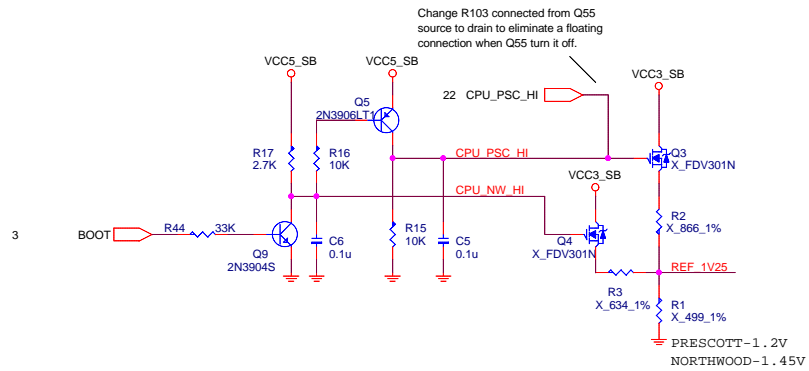
5V DUAL Power



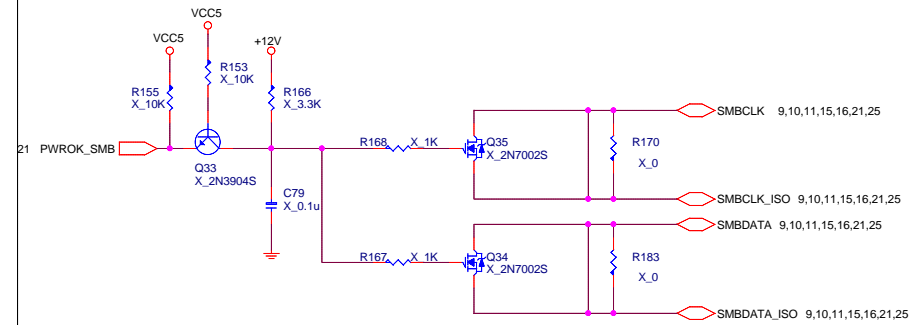
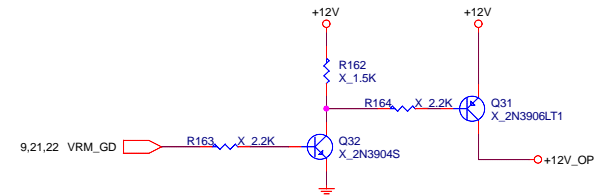
Micro-Star	Title	MS-7037	Rev	200
Document Number	ACPI Controller MS7			
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Sheet	21	of	31	



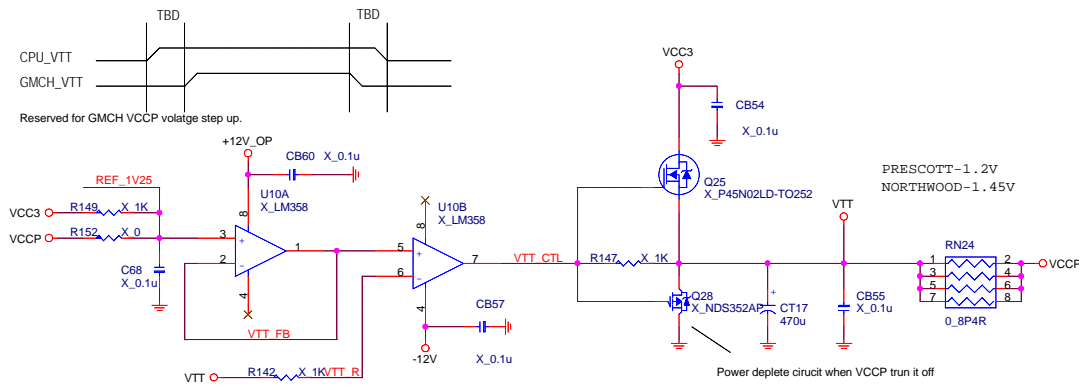
Intel reference GMCH VTT power cirucit



GMCH_VTT ON/OFF CIRCUIT



GMCH VTT Generator



Bootstrap pin are input rather then output on Intel Prescott processor, either it's internal weak pull-up but still need to identify it can be sufficient driving capability for out side ciruit. And the bootstrap pin power by core voltage so the outside circuit need to adjust the turn off voltage.

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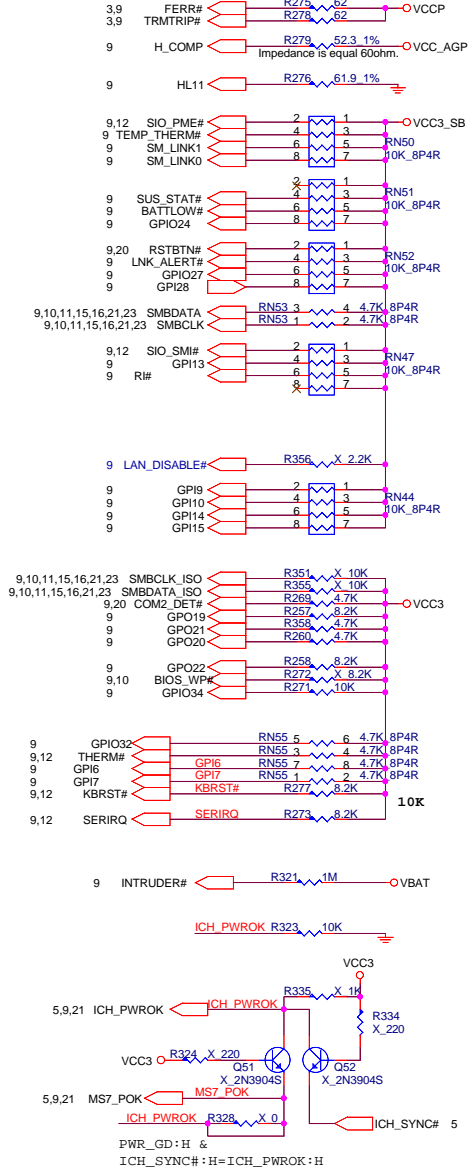
1

L

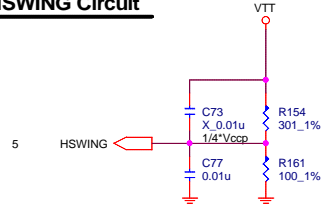
ICH5 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH5

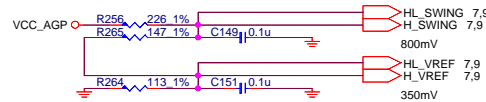
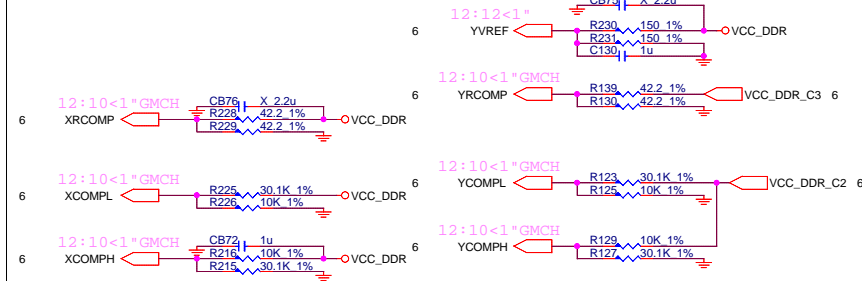
Trace length is less than 3inches to ICH5



HSWING Circuit

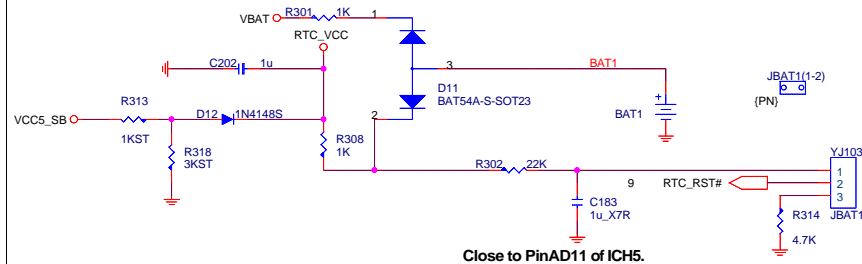


5VREF Sequencing Circuit



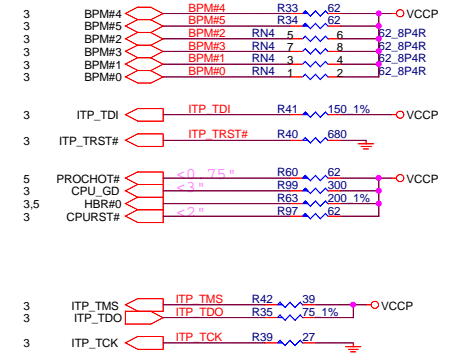
RTC BLOCK

CLR CMOS	
1-2	Normal *
2-3	Clear CMOS



CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



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ICH5

GPIO Pin	Type	Function	Power well
GPIO 0	I	PREQ#A	MAIN
GPIO 1	I	PREQ#B	MAIN
GPIO 2	I	PIRQ#E	MAIN
GPIO 3	I	PIRQ#F	MAIN
GPIO 4	I	PIRQ#G	MAIN
GPIO 5	I	PIRQ#H	MAIN
GPIO 6	I	GPI6	MAIN
GPIO 7	I	GPI7	MAIN
GPIO 8	I	SIO_PME#	RESUME
GPIO 9	I	OC4#	RESUME
GPIO 10	I	OC5#	RESUME
GPIO 11	I	TEMP_THERM#	RESUME
GPIO 12	I	SIO_SMI#	RESUME
GPIO 13	I	GPI13	RESUME
GPIO 14	I	OC#6	RESUME
GPIO 15	I	OC#7	RESUME
GPIO 16	O	PGNT#A	MAIN
GPIO 17	O	PGNT#B	MAIN
GPIO 18	O	GPO18	MAIN
GPIO 19	O	GPO19	MAIN
GPIO 20	O	GPO20	MAIN
GPIO 21	O	GPO21	MAIN
GPIO 22	OD	GPO22	MAIN
GPIO 23	O	BIOS_WP#	MAIN
GPIO 24	I/O	GPIO24	RESUME
GPIO 25	I/O	LAN_DISABLE#	RESUME
GPIO 27	I/O	GPIO27	RESUME
GPIO 28	I/O	GPIO28	RESUME
GPIO 32	I/O	GPIO32	MAIN
GPIO 33	I/O	COM2_DET#	MAIN
GPIO 34	I/O	GPIO34	MAIN
GPIO 40	I	PREQ#4	MAIN
GPIO 41	I	GPI41	MAIN
GPIO 48	O	PGNT#4	MAIN
GPIO 49	OD	CPU_GD	MAIN

default output
default output
default output
default output
default output
default output

PCI RESET DEVICE

Signals	Target
PCIRST#1	LAN,1394
PCIRST#2	Super I/O,AGP slot
PCIRST#3	PCI1~3
PCIRST_ICH5#	Northbridge , FWH
HDDRST#	Primary, Scoundary IDE

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#G PIRQ#H PIRQ#E PIRQ#F	PCI_REQ#0 PCI_GNT#0	AD26	PCICLK0
PCI Slot 2	PIRQ#F PIRQ#G PIRQ#H PIRQ#E	PCI_REQ#4 PCI_GNT#4	AD25	PCICLK1
PCI Slot 3	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PCI_REQ#2 PCI_GNT#2	AD28	PCICLK2
LAN	PIRQH	PCI_REQ#1 PCI_GNT#1	AD29	LAN_PCLK
1394	PIRQC	PCI_REQ#3 PCI_GNT#3	AD23	1394_PCLK

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

JUMPER SETTING

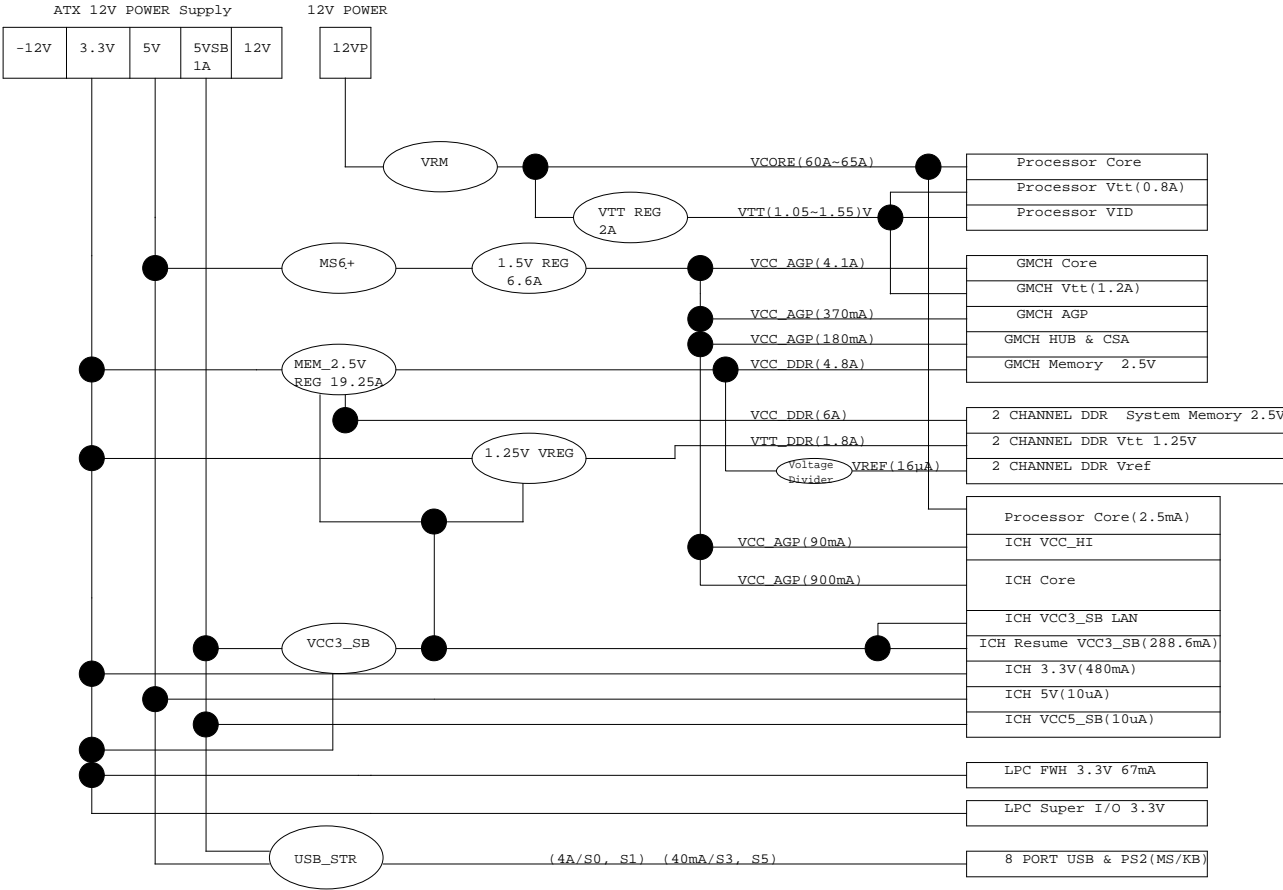
JBAT1	(1-2)NORMAL	(2-3)CLEAR
JAUD1	(5-6) (9-10) W/O FRONT AUDIO	WITH FRONT AUDIO

SIO

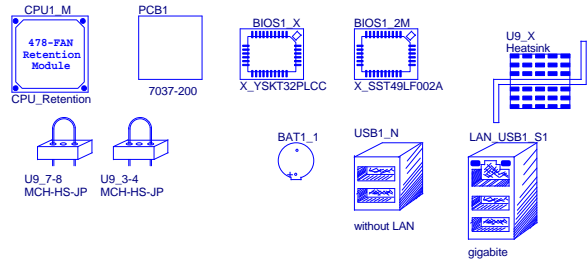
PIN NAME	USAGE	Input/Output	NOTES
GPIO10	UNUSED	INPUT	
GPIO11	UNUSED	INPUT	
GPIO12	UNUSED	INPUT	
GPIO13	UNUSED	INPUT	
GPIO14	UNUSED	OUTPUT	
GPIO15	VID5	INPUT	Low: VID add 0.0125V , High :by pass
GPIO16	UNUSED	OUTPUT	
GPIO17	UNUSED	OUTPUT	
GPIO20	UNUSED	OUTPUT	
GPIO21	SMBCLK_ISO	INPUT	SMBUS CLOCK
GPIO22	SMBDATA_ISO	INPUT / OUTPUT	SMBUS DATA
GPIO23	POWER_LED	OUTPUT	Default used MS-7
GPIO24	UNUSED	OUTPUT	
GPIO25	UNUSED	OUTPUT	IRRX
GPIO26	UNUSED	OUTPUT	
GPIO27	UNUSED	OUTPUT	
GPIO30	SLP_S3#	INPUT	S3 state indicator signal
GPIO31	PS_ON#	OUTPUT	Connector to Power Supply to turn on Power.
GPIO32	UNUSED	OUTPUT	
GPIO33	UNUSED	OUTPUT	
GPIO34	UNUSED	OUTPUT	
GPIO35	UNUSED	OUTPUT	

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POWER DELIVERY MAP



7037 PART



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Revision History (Changes from Rev 100)

Sheet	Description
11,12	Change NB from 865G to 848P and support single channel 2 DDR
24	Change PWM to Intersil 6556B